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# Design and Simulation of Switched Capacitor Based Multilevel Inverter with Reduced Components

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**ABSTRACT**

**Function of inverter is to convert DC signal to AC signal. Boost voltage and to improve the power quality and capacity with sinusoidal type waveform is obtained by use of multi-level inverter. The Multilevel inverter increases number of devices and other components, switched-capacitor (SC) units have ability to boost the input voltage considerably switched capacitor-based inverter with reduced switch is proposed in this paper without inductor and transformer operation with voltage boosting feature and inherent capacitor self-voltage balancing performing with no interference. The structure proposed in this paper is capable of producing 17 level output waveform with double voltage gain using a dual voltage source with reduced switches and other equipment's. The inverter switching pulse is modulated using PD-PWM technique, which enables a high quality output waveform.**

***Keywords***— Switched-Capacitor, Multilevel Inverter, Self-Charge Balancing, PD-PWM, Series-Parallel Connection

## I. INTRODUCTION

Most renewable energy generated in dc only, to supply or transfer this energy in dc is challenging task FACTS require inverting operation and in development of other advanced equipment's in industries requires ac signals with pure sinusoidal wave and lesser THD. Inverter is used to convert DC to AC signals, and inverter is capable to drive variable frequency and voltage drives. To improve the power quality with lower THD reduced switches stressless compatible interference, higher efficiency.

Multilevel inverters generate an AC voltage using small voltage steps obtained with help of DC supplies or capacitor bank. To achieve all above factors multilevel inverters were been used. With wide spread usage of multilevel inverter has been introduced. Diode clamped type multilevel inverter. Flying capacitor type multilevel inverter. Neutral point clamped type, modular multilevel type inverter, Cascaded H bridge type multilevel inverter are the some of the types multi-level inverter used in practice. All these types of multilevel inverter use large number of switches and switching pulse which increases complexity. With this filter are used to reduce THD and other losses which increases size and cost. Many techniques and design were been introduced to reduces the number of equipment's reduces switches counts. Multi-level inverter utilizes many numbers of dc sources, a greater number of dc sources is used to achieve high voltage levels. These topologies appear to be advantageous as power quality and density increases, but lacks in use of a greater number of switches and transformer to increases the higher voltage.

A new technique is proposed has been an excellent option to achieve higher voltage levels and maintain higher quality power density and complexity is optimized cost. Several structure have been introduced in recent years, switched capacitor, switched diode, switched source ,switched inductor these are new technologies. Among these switched diode and switched source are non-boosting type inverter, Switched capacitor is used in proposed paper with boosting techniques. In switched capacitor type single source boosting, multi-source boosting and non-boosting were been used. In attempt to reduce the number of switches count SC based multilevel inverter are used with reduced components. Since development of SCMLI has been introduced fastly in various industries, SC based units came forward as switched boost by including many activities of different design plenty of SC based were introduced ,In this proposed structure a dual source seventeen level double boost type multilevel inverter is used. which utilizes ten switches, four diode and two capacitors.

The main purpose towards SC-MLIs can be listed below.

1) Reduction in number of switches with producing maximum level number of output voltage.

2) Enhancing the overall output voltage gain using a two source.

3) Controlling the current stress/loss profile of switches through soft charging or pulse width modulation (PWM)-based techniques.

This article suggests a dual-source 17-level switched capacitor inverter that is capable of providing quadruple voltage-gain. The large boosting capability, capacitors natural charge balancing as well as fundamental frequency operation of H-bridge switches are distinguished features of suggested inverter.

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## II. PRINCIPLE OPERATION OF PROPOSED 17-LEVEL SCMLI

Fig.2.1 shows the proposed single phase 17-level SCMLI. It consisting of a dual dc sources $V_{dc}$ and ten switches(S1,S2,S3,S4,S5,S6,S7,S8,S9,S10). The circuit can be divided into three parts. It consists of two modules and a H-bridge for simplified analysis. The first module (M1) consists of two switches(S1,S2), two diode (D1,D2) and one capacitor (C1); while the second module (M2) employs two switches (S3,S4), two diodes(D3,D4) and one capacitor (C2). The M1 doubles the input voltage and M2 further boost the output of M1 to twice. The switches(S5-S10) are arranged in such a way that they can create the required ac output by avoiding the end side full bridge. As a result, the stress across the devices in M1 is Vin and all other devices withstand 2Vin stress. By maintaining a voltage ratio of 1:2 across the capacitors C1 and C2, the proposed MLI synthesizes 17-level output(0,0.25$V_{in}$,0.5$V_{in}$,0.75$V_{in}$,$V_{in}$,1.25$V_{in}$,1.5$V_{in}$,1.75$V_{in}$, 2$V_{in}$) The switch pairs (S1, S2), (S3,S4), (S5, S6) (S7, S8) and (S9,S10)operate in a complementary fashion, which result simplified circuit operation. Further, simultaneous operation of the switch combinations (S5,S6,S7) and (S8, S9, S10) are avoided to prevent short-circuiting of the source. The diode D1is forward biased only when the switch S1 is in off condition; whereas, D2 are forward biased once the switch-pair(S) is in off condition switches.

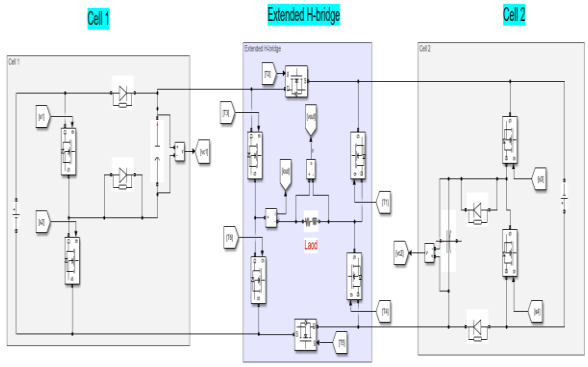


**Figure 2.1:** Proposed 17-level quadruple boost SCMLI topology

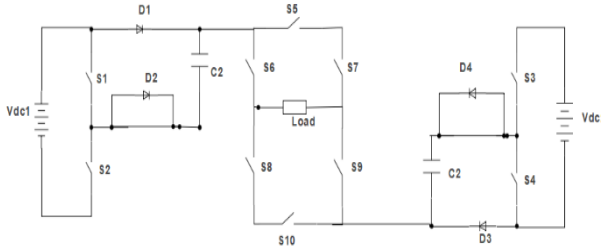


**Figure 2.2:** Proposed 17-level quadruple boost SCMLI topology

**Table 2.1**

| Voltage | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 2V | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1.75V | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1.5V | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1.25V | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1V | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0.75V | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0.5V | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0.25V | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0V | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| -0.25V | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| -0.50V | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| -0.75V | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| -1V | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| -1.25V | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -1.5V | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| -1.75V | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -2V | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

**Table 2.1:** Switching table

## III. SELECTION OF CAPACITOR VALUE

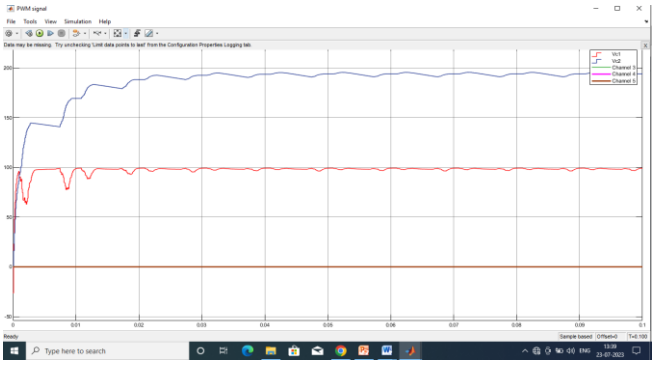

**Figure 3.1:** Charging voltage levels

During the initial half cycle as shown the capacitor is directly connected to $V_{dc}$, It is charged up to $V_{dc}$. Similarly, during the negative half cycle with voltage levels of zero and gets charged by having a parallel connection with the input dc supply. For the charging loop, the time constant RC has a value which is lower than the charging duration. This results in the full charging of the capacitor C1. During the voltage levels of and $V_{dc}$, the energy stored in the capacitor is transferred to the load. The lowering in stored the energy level causes a voltage drop in the capacitor voltage, Where as $I_{pk}$ is the peak current value of the load current, $\Delta V_c$ is the ripple voltage value and $f_o$ is the frequency of the output voltage. C1 charged up to 100V, C2 charged upto 200V.and during charging its been stored.

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## IV. MODULATION STRATEGY

For the proposed 17-level topology, phase-disposition pulse width modulation (PD-PWM) technique has been used. In these carrier frequency signals each peak-to-peak amplitude is one and frequency of Fcr were compared with a input ac sinusoidal reference signal having a peak value of Vsine to generate the pulses. Fig. 4.1 shows the sinusoidal reference signal along with carrier waveforms to achieve the seventeen levels output voltage. To generate the gate pulses for different switches and the logic for the PWM generation is depicted. The modulation index (MI) for the 17-level PD-PWM is given as sine wave the gate pulse generation based on the switching logic of the proposed topology is shown in below tables and switching frequency is shown in waveforms.

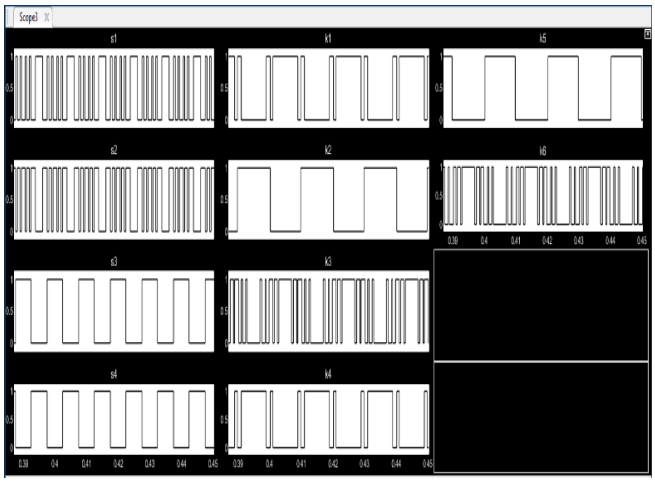

**Figure 4.1:** Switching pulse waveforms

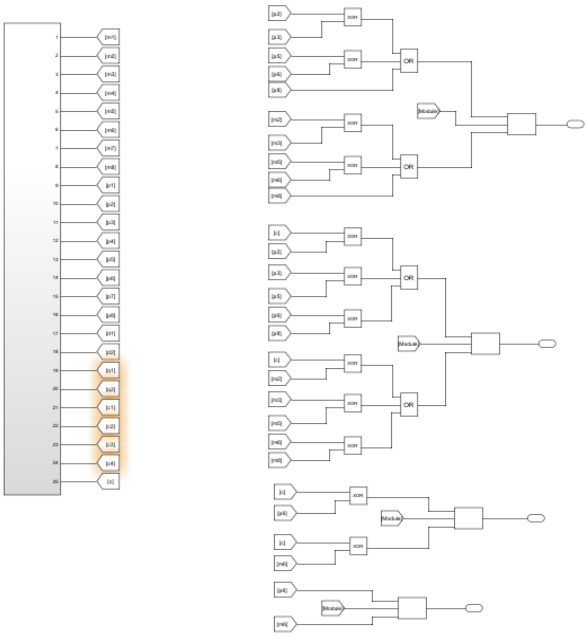

**Figure 4.2:** PD-PWM pulse generator

## V. COMPARATIVE ASSESSMENT

To appraise the dominance of the proposed 17-level SCMLI, a thorough comparison is carried out with recent-art 17-level MLIs.

**Comparison in Table 5.1**

| Parameter | $N_{DC}$ | $N_{SW}$ | $N_C$ | $N_{dd}$ | Gain | Full bridge |
|---|---|---|---|---|---|---|
| [8] | 1 | 25 | 7 | - | 2 | YES |
| [9] | 4 | 24 | 4 | 4 | 4 | YES |
| [10] | 4 | 20 | 4 | 2 | 4 | NO |
| [11] | 2 | 18 | 4 | 2 | 2 | NO |
| [12] | 1 | 39 | 7 | - | 2 | NO |
| Proposed | 2 | 10 | 2 | 2 | 2 | YES |

Where Nsw is number of switches, $N_{dd}$ is diodes, $N_{DC}$ is DC sources, $N_c$ is number of capacitors.

## VI. TEST PARAMETER

**Table 6.1:** Testing parameter

| PARAMETERS | VALUES |
|---|---|
| INPUT DC SOURCES $V_{DC}$ | 100 V,200V |
| CAPACITOR(C1 AND C2) | 3300μF (36 mΩ), 4700μF (18mΩ) |
| NOMINAL OUTPUT FREQUENCY ($F_N$) | 50 HERTZ |
| LOAD (RL) | 100Ω,40μH |

## VII. SIMULATION VERIFICATION

To validate the operability of the proposed 17-level SCMLI, simulations are carried out using MATLAB /Simulink environment and the experimental results are obtained using a laboratory-scale prototype. A. Simulation analysis. The switching pulses are obtained using the fundamental frequency switching scheme, based on pre computed angles. Using Fourier series, the 17-level staircase output waveform. The steady-state capacitor voltages ($V_{c1}$ and $V_{c2}$) are about 100V and 200V which produces a quadruple boost 17-level output. Under sudden switching of loads from no-load to UPF Fig.4.1shows the load current straight away increases without any distortion in the load voltage. Similar to the simulation result, under dynamic varying inductive loading the RMS value of the load current smoothly changes from 1.3A rms in Fig. and at the same time maintains the desired 17-level output. Under this condition, depicts the capacitor voltage ripples that decrease with an increase in the loading further verifies the inherent voltage balancing of the capacitors under the sudden drop in input voltage from 100V. The capacitor voltages are in basically settled without any auxiliary controller while maintaining the desired 17-level boost output. The efficiency and power loss analysis of the proposed 17-level SCMLI is shown in respectively under load conditions. The efficiency of the prototype is 96.94%

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under load, respectively. The active-reactive power are shown whereas, the current THD is low due to the sinusoidal-like current waveform under the inductive loading.

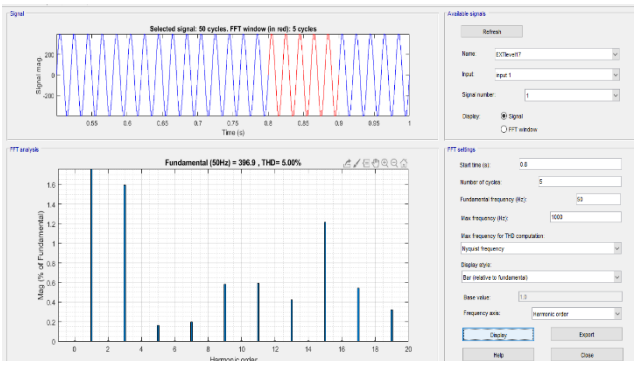



**Figure 6:** Voltage Waveform THD FFT analysis

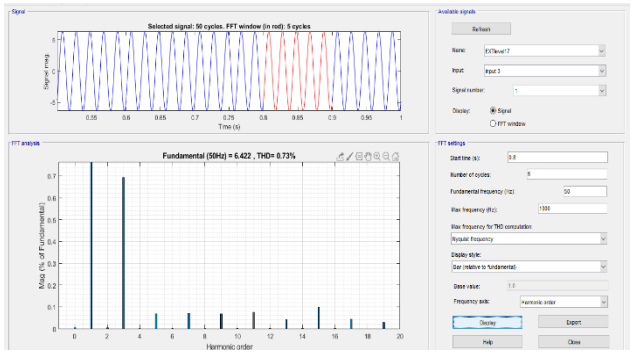
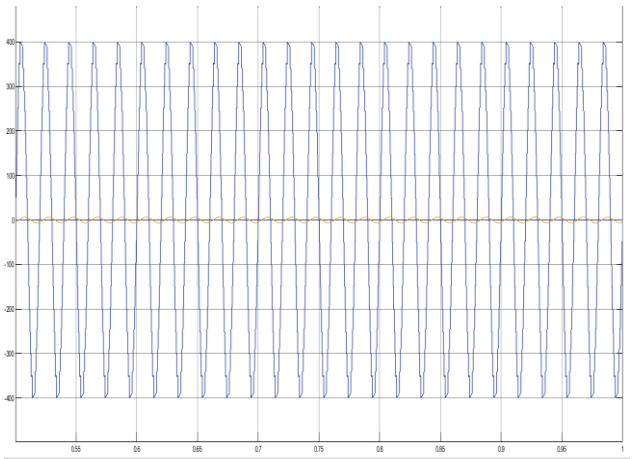
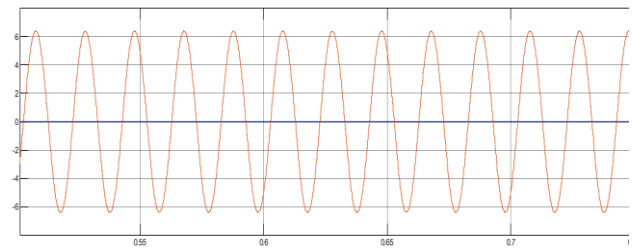



**Figure 7:** Current Waveform THD FFT analysis



X – axis time in seconds, Y axis-Voltage in volts



X – axis time in seconds, Y axis-current in amps

**Figure 8:** Waveform THD FFT analysis

## VIII. CONCLUSION

In this paper, a switched capacitor based single phase multi-level inverter with reduced number of devices is first simulated. THD voltage is 5% and current THD is 0.75%.Where in the models focus on reducing losses and costs while increasing reliability. A literature survey of the different topologies of multi-level inverters and new PWM techniques was presented. The carrier based PDPWM technique was used for generating switching pulses. The output waveforms for voltage and current were recorded for a resistive load. Simulation was done in MATLAB Simulink environment using the Sims cape Power Systems toolbox. FFT analysis for output voltage and current was done and the THD was noted. The proposed topology has been simulated using PD-PWM modulation techniques.

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