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AMS SoC Formal Verification based on Hybrid Scheme

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ABSTRACT

This paper proposes for AMS SoC formal verification based on Hybrid Scheme combined with symbolic computing and LHPN model, FV-HS. The paper is concerned with a class of AMS designs, continuous-time AMS designs i.e., tunnel diode oscillator for research target. Firstly, Labeled Hybrid Petri Net model is established for safety property verification of tunnel diode oscillator, then mathematical expression for this model is extracted for efficiency enhancement, and then proof policy built in computer algebra Maple is applied to the corresponding LHPN model for tunnel diode oscillator to verify the property. The proposed method is implemented on tunnel diode oscillator and experiment results demonstrate the advantages of the proposed method over previous method. The proposed method overcomes the drawbacks of LHPN, makes full use of the merits of LHPN and symbolic computing, simplifies the workflow of algorithm and enhances the efficiency.

Keywords— AMS SoC, Formal verification, Labeled Hybrid Petri Net, Symbolic computing

I. INTRODUCTION

Embedded components are becoming core in a growing range of electronic devices. Cornerstones of embedded systems are analog and mixed signal (AMS) designs, which are integrated circuits indispensible at the interface between electronic system and the real world environment. Analog circuit helps to secure the correct and steady operation of system. It follows that AMS design has become the necessity in people's daily life. Therefore formal verification for AMS design is extremely important for SoC design and account for the most efforts and time of the IC designers. These AMS circuits are mostly used in safety-crucial systems such as communication vehicles, ABS system etc. Research materials show that nowadays of 75% circuits are AMS circuits, while 50% faults occur on analog part [1]. Therefore it is increasingly important for designers to ensure the correctness of AMS circuit design. Formal verification is among the techniques to secure the correctness of AMS design.

Checkmate developed by CMU researchers is used to verify diode oscillator and Σ-Δ demodulator, and d/dt is applied to verify bi-quadratic low pass filter [2-5]. Discrete analog transition structure (DATS) is proposed by Sebastian to accurately express optimization of nonlinear analog circuit. The accuracy of the proposed model is close to instant analysis with less number of states. The corresponding algorithm for formal verification of AMS SoC maps the partition into DATS. Such method is able to detect the errors hidden in circuit design [6]. Labeled Hybrid Petri Net (LHPN) is developed for formal verification of AMS design [7]. LHPN outperforms pervious methods in that previous ones mostly require the designers to master hybrid automaton or hybrid Petri Net for AMS description, and they does not necessarily follow the rigid Hardware Description Language requirements; with LHPN, the designers can describe the AMS circuits of interest using their familiar language therefore LHPN becomes more popular and universal. LHPN can deal with heterogeneous components of AMS system, e.g. the analog parts and digital parts. In [8], a novel method of symbol computing is proposed for property verification of AMS design. The major idea is to verify AMS design using the same way as SAT, BDD based formal verification for digital system, to verify system automatically. This paper describes a novel verification frame work for the verification of AMS SoC that support intervals on the rates of change for the continuous variables. The proposed method begins with a model of the AMS SoC described using LHPN. VHDL-AMS allows the designers to use it to describe AMS SoC and the description is compiled into

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LHPN automatically. Then maple inbuilt proof policy is utilized accordingly for further property verification for tunnel diode oscillator. If the property is verified then the proposed algorithm terminates, otherwise a counter-example against the design model can be obtained, then the verification is complete and a failure is reported.

II. LHPN MODEL DESIGN

Figure 1 shows an LHPN model for the tunnel diode oscillator, when the circuit is launched, the tunnel diode oscillator is experiencing transition period from event p_1 to node N_1 from initial node N_0, then such token is removed from the preset for transition period p_1, added to the post set for transition period p_1, when system transit from event p_2 to node N_2, the token is removed from the preset of places for transition period p_2, added to the post set of places for it, and system transits period from event p_3 to node N_3, token is removed from preset of places and added to post set of p_3, and then remains in node N_3 therefore oscillating behavior cannot be accomplished. While in Figure 2, starting from one node, tunnel diode oscillator transits period from p_1, p_2 and p_3 sequentially to conduct behavior of oscillating.

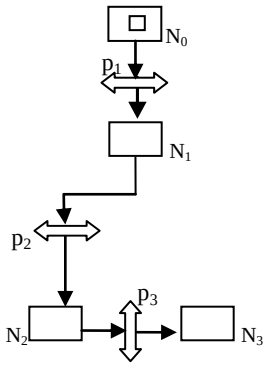

Figure 1: LHPN model for TDO non-oscillating node

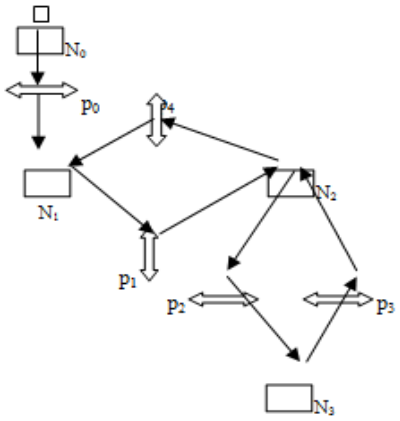

Figure 2: LHPN model for TDO oscillating node

III. RESULT SUMMARY

Table I shows the experimental results comparison among PHAVer [8], LHPN [6] and the proposed method. The parameters used for the experiment stems from [2]. The initial conditions are $I_l \in [0.4,0.5]$ mA,Vc∈ [0.4,0.5]v. Our verification aims at modeling for oscillating behavior and non-oscillating behavior of tunnel diode oscillator using 16-bit discrete regions under specific circuit parameters and initial conditions. When R = 200Ω, LHPN model uses 14.62s for property verification. 17703 state sets are found in 14.62s when R = 242Ω, 1826 state sets are found in 0.34s when R = 242Ω. We tried to use tool HYTECH for the verification without success due to overflow errors. PHAVer model checking accomplish oscillating property checking for tunnel diode oscillator within 72.8s, however the proposed method only takes 11.93s, hence achieves higher efficiency than that in [6].

TABLE I
COMPARISONS ON TUNNEL DIODE OSCILLATOR

Approach	PHAVer[8]		LHPN[6]		Proposed	
Instance	Time(s)	OK?	Time(s)	OK?	Time(s)	OK?
TDO (non-oscillating)	N.R.	N/A	0.34	No	0.31	No
TDO (Oscillating)	72.8	N/A	14.62	Yes	11.93	Yes

IV. CONCLUSION

This paper describes the formal verification for AMS SoC, FV-HS tunnel diode oscillator is taken for instance for formal verification of AMS SoC. The proposed method has been applied to tunnel diode oscillator; it can be automatically integrated into the application flow and overcomes the limits of bounded time for exhaustive method. The proposed method achieves low complexity and high efficiency.

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