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Improvement of Power Factor and Harmonic Reduction with VSC for HVDC System

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ABSTRACT

This paper deals with analysis, simulation and control of a two level 48-pulse voltage source converter for High Voltage DC (HVDC) system. A set of two-level 6-pulse voltage source converters (VSCs) is used to form a 48-pulse converter operated at Fundamental Component of Switching Frequency (FCSF). The performance of the VSC system is improved in terms of reduced harmonic level at FCSF and THD (Total Harmonic Distortion). The performance of the VSC is studied to improve power factor and reduce harmonic distortion. Simulation results are presented for the proposed two level multi pulse converter.

Index Terms – Two-Level Voltage Source Converter, HVDC Systems, Multi pulse, Fundamental Frequency Switching, Harmonics,

I. INTRODUCTION

HVDC schemes employing line-commutated, current source converter using thyristors have been widely used in power transmission. The control schemes for such systems are well established and operating successfully all over the world [1]. Voltage Source Converter (VSC) based HVDC systems using self commutated device technology has attracted increasing attention and a number of installations are now in operation all over the world transmitting more than 70,000 MW power [1]. One of the principle advantages of VSC HVDC system is that no external voltage source required for commutation. It can independently control the reactive power flow at each AC network, and reactive power control is independent of the active power control. These features make the VSC based HVDC system attractive for connection of weak AC systems, island networks and renewable sources to a main grid [2]. A VSC based HVDC system uses a basic three phase 6-pulse voltage source converter bridge as its main unit. This VSC bridge is forced to operate at very high switching frequency in order to minimize the effect of harmonics in the system. Therefore, VSC in HVDC system has high power loss and high cost compared to conventional HVDC system [3]-[4].

HVDC conversion is implemented mostly by mono polar or bipolar configurations of 12-pulse series connected thyristor converters. In such a case the resulting high contents of 12- pulse converter related harmonics can couple into nearby telephone lines and cause noise in the communication network. This may also cause mal-function of protective relaying and circuit breakers [5]. To avoid such undesirable harmonic effects, tuned passive filters have been employed on the AC side of the converter. To reduce the harmonic distortion in VSC based HVDC systems without using conventional filters, there are three feasible solutions. These are through the use of multi-pulse converter, the multi-level converter, and the pulse width modulation (PWM) technique. The PWM converter should switch many times within one power cycle to synthesize its output waveform, therefore its switching loss is reasonably high, and this greatly limits its development in high power applications. Magnetic coupled multi pulse converter has two or more bridges and develops the staircase voltage waveform by varying transformer turns ratio with zigzag connections [5].

In these multi pulse converter circuits the converter bridges are operated at fundamental frequency switching (FFS) thus reduce the switching losses substantially. Pulse number can be increased in multiples of six, and an increase in every six pulse VSC reduces the harmonics in the system proportionally. The THD of stepped voltage of two level multi pulse VSC converters are given in Table I. From this table, it is clear that VSC only with pulse number 48 qualified the IEEE standard 519, where the THD is less than 5%. A 48- pulse voltage source converter is already reported for STATCOM applications [7]. This paper proposes a 48-pulse voltage source converter (VSC) for HVDC system. The reason for choosing 48-pulse operation in this work is that a 48-pulse voltage source converter will give THD within IEEE 519 standard compared to other pulse number such as 30 and 36 as shown in Table I.

Pulse number	6	12	18	24	30	36	42	48	96
% VSC voltage THD	30.9	15.2	10.1	7.5	6.1	5.4	4.3	3.75	1.8

TABLE I
STANDARD VOLTAGE THD OF TWO-LEVEL MULTIPULSE CONVERTERS

The control of proposed 48-pulse voltage source converter is demonstrated and validated for HVDC system. The results show a substantial reduction in voltage and current harmonics and THD is well controlled within the limit of IEEE 519 standard. This 48-pulse voltage source converter is demonstrated a potential candidate for high power and high voltage AC-DC conversion with minimum switching losses and reduced voltage and current THDs.

II. CONVERTER SYSTEM CONFIGURATION

Fig. 1 shows the circuit configuration of a 48-pulse voltage source converter based back-to-back HVDC system. Eight two-level converters are used in this configuration. In this work the rectifier operation is simulated by considering resistance as an equivalent of an inverter. These converters are connected in parallel at the dc side. The HVDC system is rated for 100 MW with an each unit of 12.5 MW. It uses common dc link capacitors. Total of (8X6) 48 solid state switching devices are used on each side converter system. The DC link voltage can be selected according the system configuration by appropriate turns ratio of the converter transformer. For back-to-back HVDC system it can be designed for low DC link voltage. The HVDC system is modeled as eight units of 6- pulse converters that are connected in parallel with appropriate phase shift to achieve the 48 pulse converter operation. Each 6-pulse converter uses a set of Y/ZZ transformers connection for phase shift. The transformers are designed to give a phase shift of 7.5q between two adjacent 6-pulse converters. The phase shift value is chosen in such a way to have an identical transformer design. This reduces the magnetic losses in transformers. Transformers secondary windings are connected in Y configuration. The primary windings of these transformers are connected in series and these consist of zigzag connections. The zigzag connection is used as a phase shifting winding and gives the phase shift of 7.5q between the two adjacent 6- pulse converters. Appropriate phase shift is also introduced in the gate pulses of an individual converter signal [8]. The net 48-pulse converter AC output voltage is given by

$$V_{ab48}(t) = 8\{V_{ab1}\sin(\omega t + 30^\circ) + V_{ab47}\sin(47\omega t + 150^\circ) + V_{ab49}\sin(49\omega t + 210^\circ) + V_{ab95}\sin(95\omega t + 330^\circ) + ...\} \quad (1)$$

This converter behaves as a 48-pulse converter where the minimum harmonics are of the order 47^{th} and 49^{th}. This converter generates an almost equivalent to sinusoidal waveform consisting of stepped waveform equivalent to a 48-pulse converter and THD of voltage and current is well maintained within IEEE 519 standard and qualify for the application in HVDC system without using PWM technique where the switching loss is quite high. The synthesis of sinusoidal waveform using the stepped waveform is shown in Fig. 2**.** The system parameters used for the simulation are given in Appendix.

III. CONTROL ALGORITHM

The objective of the control algorithm of VSC is to maintain the DC voltage at the given reference value and to control the active power flow from AC grid to DC side, along with supplying required reactive power to the AC mains. A set of capacitors is used at the DC bus to support the DC bus voltage at the required value to make the real power balance between the two sides of the converter, which is most important for the successful operation of the VSC based HVDC system. The stored energy in the capacitors reduces or increases if the active power is not balanced between two sides of converter stations. It consists of two controllers, one is the DC voltage controller and other one is the current controller [9].

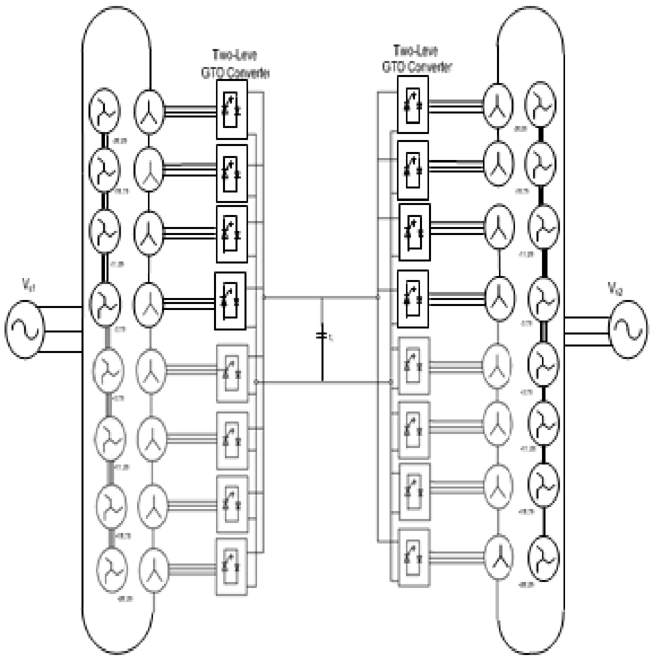


Fig. 1 A 48-Pulse voltage source converter based HVDC system configuration

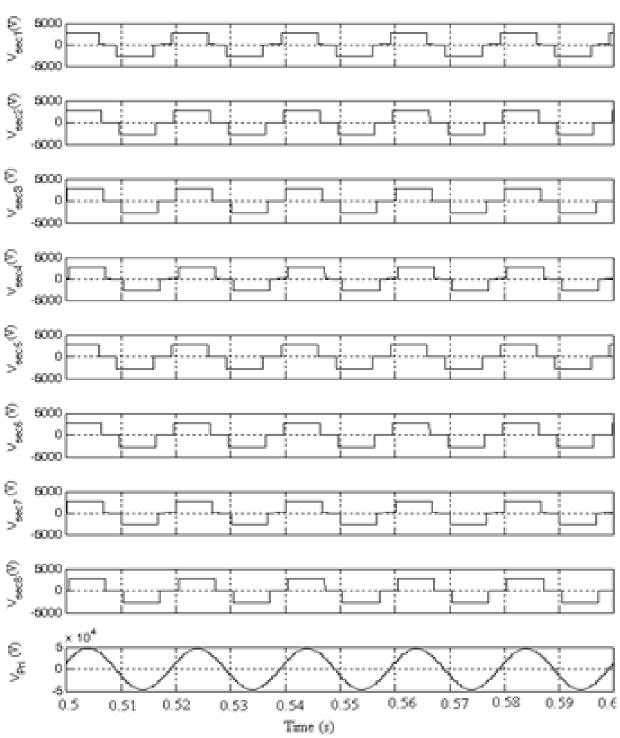


Fig. 2 Synthesis of Stepped AC voltage waveform of 48-pulse VSC.

A. DC Voltage Controller

The DC voltage controller is shown in shown in Fig. 3a in which reference currents (i_d*, i_q*) are achieved by the DC voltage controller from the reference real power and reference DC voltage as given below [10]

$$i^*_d = (P^* / V_s) + K_V (V^*_{dc} - V_{dc}) \quad (2)$$

$$i^*_q = (Q^* / 3V_s) \quad (3)$$

where P^* is the reference real power to be transmitted from one side to another side, K_V is proportional gain constant, V_s is rms supply voltage, and V^*_{dc} is reference DC voltage. The reference value of the reactive current (I_q) is supplied directly to the inner current loops and is regulated equal to zero in this study. The first term in (2) decides the power flow in the system and second term achieves DC voltage regulation by means of controlling the additional amount of active power flowing from AC side to DC side. When V_{dc} is lower than the V^*_{dc}, then i^*_d is increased as shown in (2), so that a small amount of additional active power flows into the DC link capacitor through rectifier, thus V_{dc} rises up to V^*_{dc}. When V_{dc} is higher than the V^*_{dc}, then i^*_d is decreased so that the amount of active power flowing into the DC link capacitor is reduced, thus V_{dc} is lowered to V^*_{dc}.

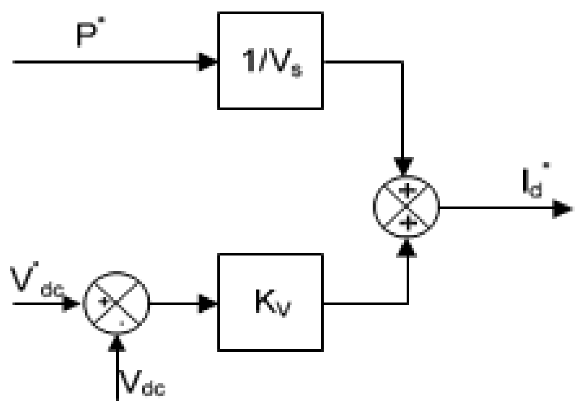


Fig.3a DC voltage controller

B. Decoupled Current controller

The decoupled current controller shown in shown in Fig. 3b. The output of the DC voltage controller is fed to the current ontroller. The voltage and current relation of the converter is given by

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} - \begin{pmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{pmatrix} = (R + L_1 \frac{d}{dt}) \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \quad (4)$$

Three phase to two phase transformation can be applied to (4) as

$$\begin{pmatrix} R+L_1\frac{d}{dt} & w_1L_1 \\ -w_1L_1 & R+L_1\frac{d}{dt} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix}=\begin{pmatrix} v_d-v_{1d} \\ v_q-v_{1q} \end{pmatrix} \quad (5)$$

Here v_{1d}, v_{1q} are the d-axis and q-axis components of v_1, while i_d, and i_q are the d-axis and q-axis components of i_s. v_d is the d-axis component of v_s whereas v_q is always zero because the supply voltage vector is aligned with the d-axis. The instantaneous active power P, and the reactive power Q are drawn from the utility grid as

$$P = V_d.i_d + V_q.i_q \quad (6)$$

$$Q = V_d.i_q + V_q.i_d \quad (7)$$

The control of i_d and i_q decides P and Q independently. This decoupled current control is applied to the system in order to achieve an independent control of i_d and i_q. The AC voltage commands in the d and q axes, are as v_d*, and v_q*. The inner current controller includes a feedback PI-controller. The reference currents (i_d*, i_q*) from dc voltage controller are given as inputs to the current controller, and these provide reference voltages (v_d*, v_q*). The operation of the current controller can be explained by using (8) and (9) as

$$V_d* = V_d - (R.i_d + \omega L.i_q) - \{K_{p1}(i_d * - i_d) + K_{11}\int (i_d * - i_d)d\ \} \quad (8)$$

$$V_q* = V_q - (R.i_q + \omega L.i_d) - \{K_{p2}(i_d * - i_d) + K_{12}\int (i_d * - i_d)d\ \} \quad (9)$$

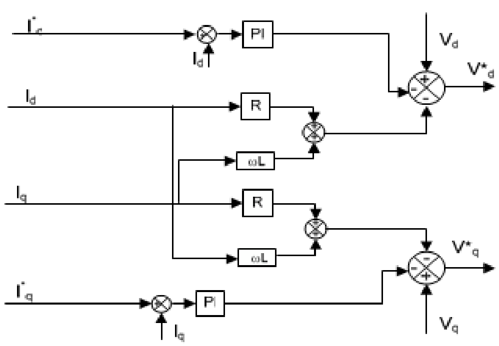


Fig.3b Decoupled Current controller

where K_{p1} and K_{p2} are proportional gain, K_{I1} and K_{I2} are integral gain, i_d, v_d and v_q are d-q values of supply voltage v_s, and i_d, i_q are d-q values of the supply current (i_s). Here i_d* and i_q* are the current commands in the d and q axes. The first and second terms of the right hand side cancel the steady state voltage appearing across the AC-link inductor L_1. The third term constitutes feedback control loops of the currents i_d and i_q. The phase shift is calculated by using the (10) as

$$\delta * = \tan^{-1}\left(\frac{v_q *}{v_d *}\right) \quad (10)$$

where $\delta *$ is the angle at which the converter devices are gated. It is the phase shift angle from the fundamental supply voltage.

IV. MATLAB BASED SIMULATION

The proposed two-level 48-pulse converter is simulated in the MATLAB environment with Simulink and Power System Block set (PSB) toolboxes. Fig. 4a shows the MATLAB model of two-level 48-pulse converter and Fig. 4b shows the transformer and converter connection to realize 48-pulse converter model. In this model, eight two-level GTO VSC bridges are used and connected in parallel in the DC side. The control algorithm is implemented using Simulink blocks. Three phase supply of 33kV, 50 Hz is connected to the converter through an interfacing reactance with a value of 0.2 pu.

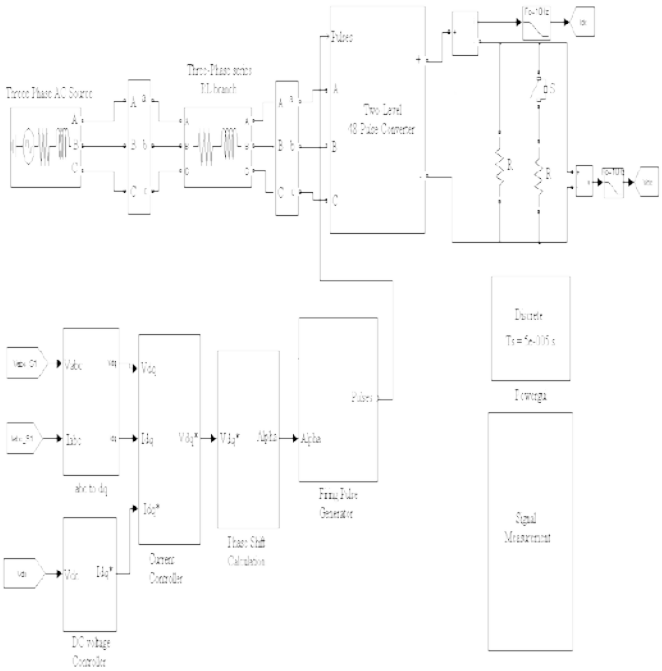


Fig. 4a MATLAB model of two-level, 48-pulse VSC system

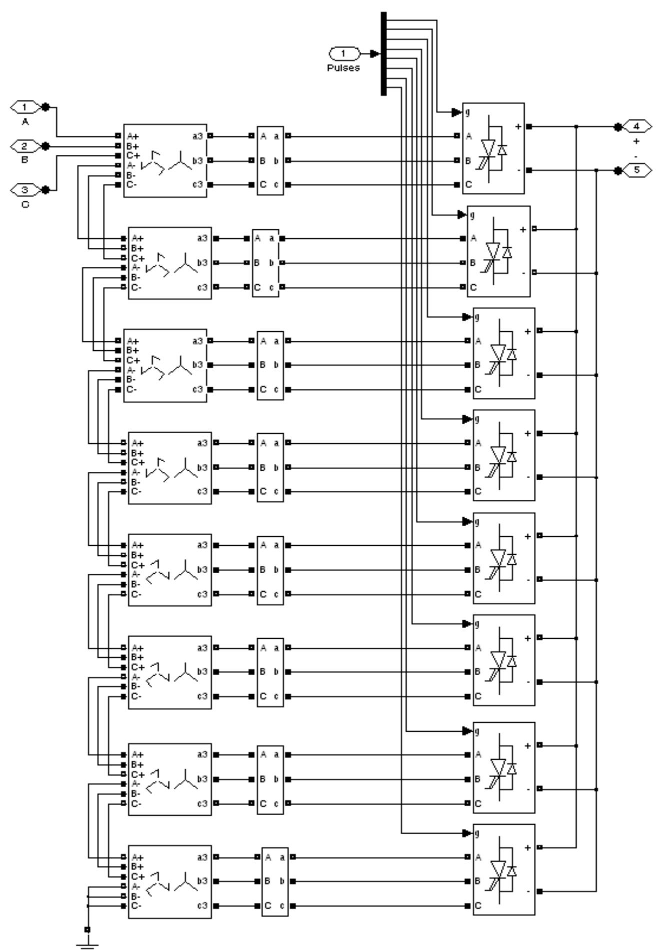


Fig. 4b MATLAB model of two-level, 48-pulse voltage source converter

and transformer

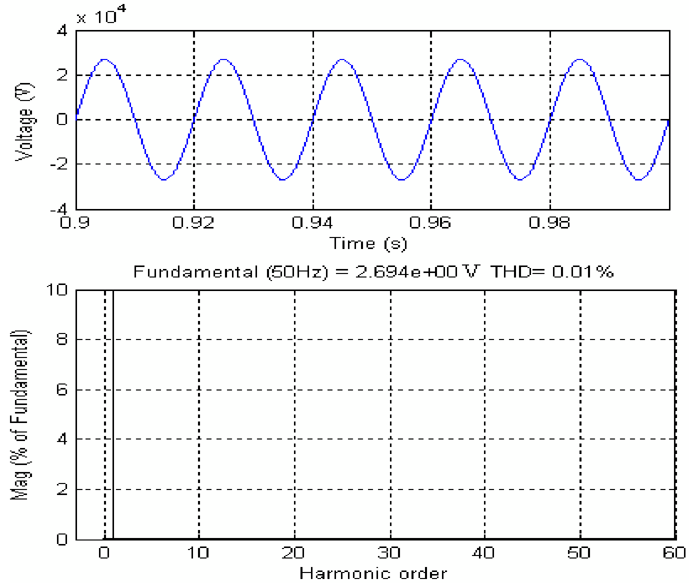
The primary windings of the transformer are connected in series therefore, the total supply voltage is shared equally by eight series connected primary windings of the transformer.

Three phase AC input is fed to the bridge through an interface reactance. The voltages at the two side of the reactance and the voltages at the two sides of the transformer are measured as supply and converter voltages. A DC capacitance is used to store energy at the DC bus.

V. RESULTS AND DISCUSSION

The steady state performance and dynamic behavior of the proposed two level, 48-pulse voltage source converter are simulated to demonstrate its capability. Fig.5 shows the steady state behavior of modeled converter system. In this figure, it shows the nature of the supply voltage (v_{abc}), ac mains current (I_{abc}), voltage (v_{pri}) and current (I_{pri}) at the primary side of the converter transformer and voltage (v_{sec}) at the input of the converter, real power (P) drawn from supply, reactive power demand (Q), DC voltage (V_{dc}), an angle delta (G) for required power flow and DC power (P_{dc}) during steady state is shown to demonstrate its behavior. The reference power command is set at 100 MW throughout the steady state operation. The phase voltage and phase current are in phase with each other as the reactive power is maintained to zero. Fig. 5 also shows the voltage and current at supply side, at the primary side of the converter transformer and at the input of the converter. Voltages reflected at the input of the converter due to switching operation are square wave in nature according to the switching pattern of the converter.

All the secondary voltages are added up and reflected voltage on the primary side of the transformer is a 48-pulse converter stepped voltage waveform almost equivalent to sinusoidal waveform. This voltage becomes smooth at the supply side due to the addition of phase shifted voltages. Harmonics spectra of a 48-pulse converter voltage waveform at the primary winding of the transformer are shown in Fig. 7, which is very close to sinusoidal waveform made up of stepped waveform with a THD of 2.9% only. The THD of converter voltage observed here for 48-pulse operation is much less than the value shown in the Table I, this is because of the value of interface reactance. The AC current is equally shared by the number of converters as they are identical in nature. Fig. 6 shows the dynamic behavior of the converter system, where the dynamic condition is introduced in the system by changing the power flow. Initial reference power is set at 75 MW and at 1s, the reference active power is increased to 100 MW. The controller responds immediately for the change in the system condition to bring back the system DC voltage to its reference value. The change in power flow is accompanied by changing the angle delta (G) and keeping all other parameters of the system remain unchanged. In Fig. 7 it may be observed that the THD of voltage is as 0.01% and THD of current is found as low as 0.43%, at 100 % active power. This shows that the converter results in low THD in current below the IEEE standard 519 [6]. This makes the supply voltage and current almost free from harmonics. Various harmonics spectrum shown in Fig. 7 is observed during steady state condition and at full load power.



(a)

Fig. 5 Steady state performance of proposed 48-pulse voltage source converter

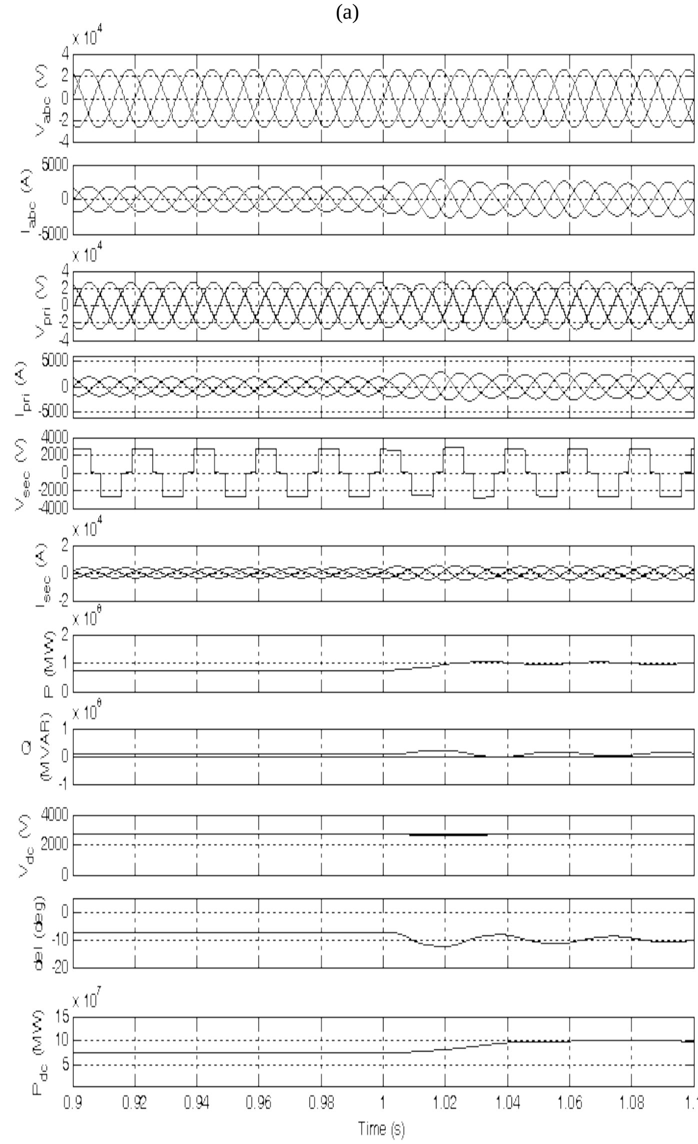
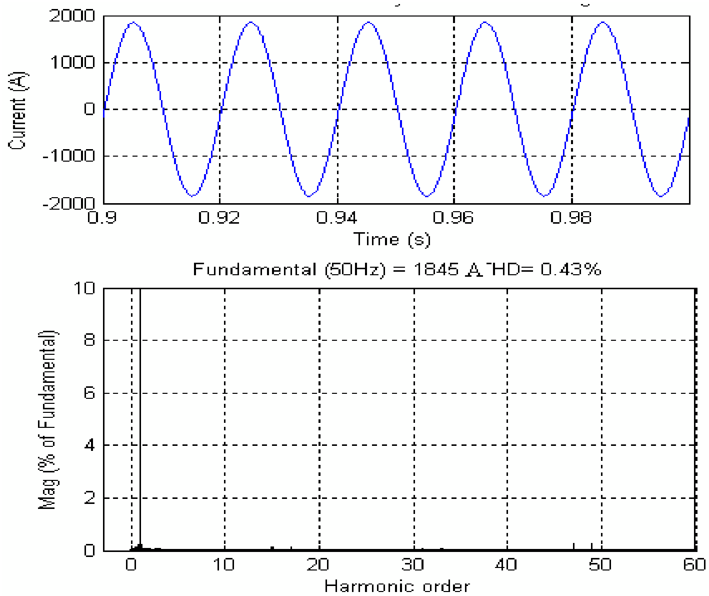
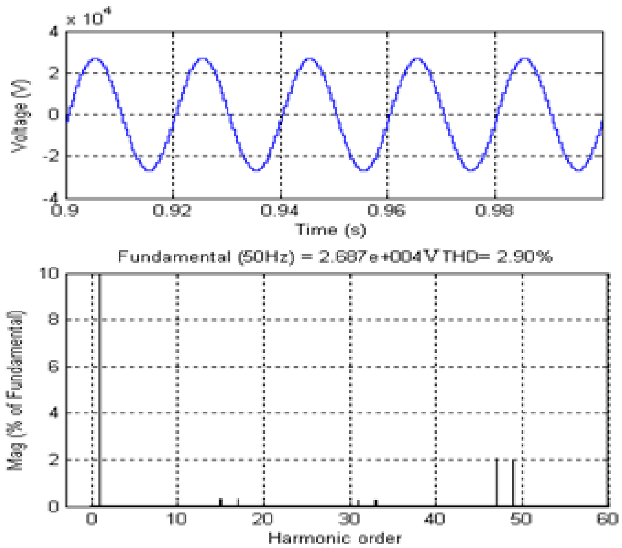


Fig. 6 Dynamic performance of proposed 48-pulse voltage source converter



(b)



(c)

Fig. 7 Waveforms and harmonic spectra of 48-pulse coverter (a) supply voltage (b) supply current (c) converter voltage

VI. CONCLUSION

A 48-pulse two-level voltage source converter has been developed and controlled for HVDC system. The transformer connections with appropriate phase shift have been used to form a 48-pulse converter. The operation of the proposed converter configuration has been simulated. The power factor is improved and harmonic distortion is reduced for the proposed converter configuration.

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